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Nonvolatile Memory Functionality of ZnO Nanowire Transistors Controlled by Mobile Protons

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ABSTRACT We demonstrated the nonvolatile memory functionality of ZnO nanowire field effect transistors (FETs) using mobile protons that are generated by high-pressure hydrogen annealing (HPHA) at relatively low temperature (400 °C). These ZnO nanowire devices exhibited reproducible hysteresis, reversible switching, and nonvolatile memory behaviors in comparison with those of the conventional FET devices. We show that the memory characteristics are attributed to the movement of protons between the Si/SiO_2 interface and the SiO_2/ZnO nanowire interface by the applied gate electric field. The memory mechanism is explained in terms of the tuning of interface properties, such as effective electric field, surface charge density, and surface barrier potential due to the movement of protons in the SiO_2 layer, consistent with the UV photoresponse characteristics of nanowire memory devices. Our study will further provide a useful route of creating memory functionality and incorporating proton-based storage elements onto a modified CMOS platform for FET memory devices using nanomaterials.

KEYWORDS: ZnO nanowires · field effect transistors · nonvolatile memory · mobile protons

The control and design of electronic properties in nanomaterial-based devices are of great importance not only for creating and exploring their novel electronic functions but also for their applications in several diverse fields, including electronics,[1] photonics,[2] chemical/biological sensing,[3,4] and solar energy conversion/storage.[5] So far, to this end, a variety of strategies have been investigated by doping,[6] heterostructure design,[7] irradiation engineering,[8] molecular functionalization techniques,[9] and interface engineering.[10,11] In particular, the interface manipulation of semiconductor devices has attracted significant attention because the operating principles and performance of these devices are critically affected by their interfacial properties.[11,12]

Most importantly, nanoscale FET configurations provide a general platform to individually functionalize the surfaces of nanomaterial species within a nanoscale system. Such a transistor configuration encompasses a large surface-to-volume ratio, and the interfaces play a crucial role in defining the fundamental transport characteristics of these transistors, especially in regard to novel memory characteristics.[12−25] For example, the electrical transport behavior or the threshold voltage of nanoscale FETs can be tuned by controlling the interfacial properties through several methods, such as surface-architecture-controlled ZnO nanowire growth,[13] proton-irradiation-assisted manipulation,[14,15] and mechanical strain.[16,17] In addition to tuning the fundamental FET properties, considerable efforts have been devoted to addressing the issues of creating memory functionality by forming functional interfacial areas through the use of electric double layers,[18] nanoparticles,[19] self-assembled molecules,[9,20] ferroelectric dielectric films,[21−23] and, particularly, mobile protons;[18,24,25] however, with regard to memory devices with mobile protons, the existing proton-generating approach at high temperatures (~1000 °C) can seriously induce undesirable effects on the materials and devices. Accordingly, the generation of mobile protons necessitates a low-temperature process as one of the key issues for the proton-based memory elements with an FET configuration.[18,24,25] Furthermore, for the wide application of the nanomaterial-based FETs beyond the FET generic function, manipulation of the interfacial properties through mobile protons for creating memory functions is very important. To the best of our knowledge, no previous work has demonstrated the nanomaterial-based memory transistors by using mobile protons generated particularly at the low temperature.

Herein, we have demonstrated that ZnO nanowire-based FETs have memory-

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switching characteristics using mobile protons, which can be generated through a high-pressure hydrogen annealing (HPHA) at a relatively low temperature (400 °C). Our primary focus is to translate the generic FET function of the ZnO nanowire transistor into memory characteristics by employing mobile protons in the SiO_2 layer. We have observed that reversible memory characteristics are attributed to proton movement between the Si/SiO_2 interface and the SiO_2/nanowire interface. Specifically, the memory characteristics of ZnO nanowire FETs can be described in terms of the effective electric field, surface charge density, and surface barrier potential at the nanowire surface, all of which depend on the movement of protons by the application of a gate electric field.

RESULTS AND DISCUSSION

A fabrication scheme of a memory device based on a single ZnO nanowire FET and its field emission scanning electron microscopy (FESEM) image are illustrated in Figure 1. First, a 50 nm thick poly-Si film was deposited onto a highly doped p-type Si substrate with a thermally grown 100 nm thick SiO_2 layer by low-pressure chemical vapor deposition (LPCVD) (Figure 1a). Next, hole patterns with diameters of 100 μm were formed in the poly-Si film for the lateral diffusion of hydrogen molecules by photolithography and wet chemical etching using a mixed solvent of HNO_3/HF/DI water (Figure 1b).[24] After the HPHA process (400 °C, 10 atm) of the patterned substrates for ~40 min (Figure 1c), the patterned poly-Si film was removed by KOH solution at 70 °C (Figure 1d). Subsequently, the ZnO nanowires grown by a vapor transport method were transferred to the Si substrates, and the FET devices were fabricated by photolithography and a lift-off process (Figure 1e). Figure 1f shows an FESEM image of a fabricated single ZnO nanowire FET device with a space of approximately 3 μm between two electrodes. Further detailed information of device fabrication is provided in the Experimental Methods.

A series of transfer characteristics (drain current *versus* gate voltage curves, $I_{DS}-V_G$) and their corresponding memory hysteresis window were measured in an ambient atmosphere and at room temperature for the nanowire memory FET devices treated with HPHA (Figure 2a−c) and for the conventional nanowire FET device without the HPHA treatment (Figure 2d−f), respectively. The transfer curves in Figure 2a,d show the direction and hysteresis behavior with a double sweep of the gate voltage (V_G) from −15 to 15 V at variable drain voltages (V_{DS} = 0.1, 0.4, 0.7, and 1 V). Figure 2b,e shows the variation of the hysteresis memory window at the various sweep ranges of V_G at a fixed drain voltage (V_{DS} = 0.1 V). Interestingly, the nanowire memory FET devices exhibited a completely different behavior in comparison to the conventional nanowire FET devices. Specifically, the memory window of the nanowire memory FETs significantly increased with increasing

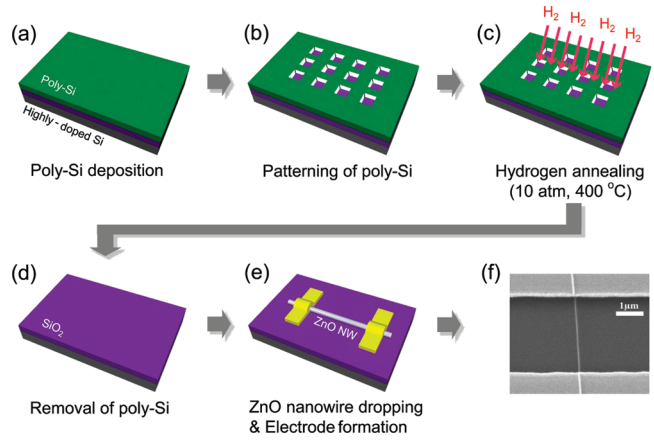

Figure 1. Fabrication process of a nanowire memory FET device. (a) The deposition of a 50 nm thick poly-Si film on a SiO_2 layer. (b) Hole patterning in the poly-Si film. (c) Hydrogen annealing at 400 °C and 10 atm. (d) Removal of the poly-Si film. (e) The fabrication of a ZnO nanowire FET device. (f) An FESEM image of a fabricated device.

gate voltage sweep ranges, whereas the conventional FETs did not exhibit any noticeable hysteresis behavior in their $I_{DS}-V_G$ characteristics. To allow for statistical descriptions of the hysteresis width as a function of the V_G sweep range, a total of 14 nanowire FET devices were characterized: 7 devices for the nanowire memory FETs (Figure 2c) and 7 devices for the conventional nanowire FETs (Figure 2f). The hysteresis widths of the nanowire memory FET devices exhibited much stronger linear dependence on the V_G sweep range than those of conventional FET devices. The hysteresis widths of the

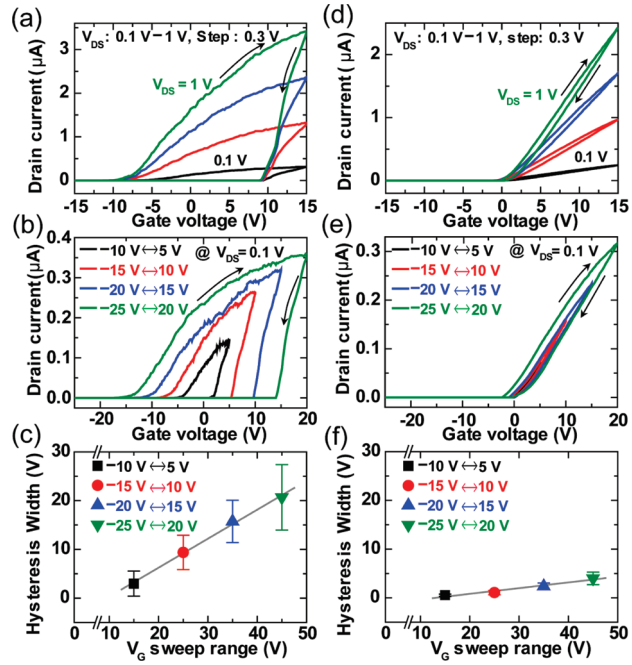

Figure 2. Electrical characteristics of (a−c) the nanowire memory devices and (d−f) the conventional nanowire devices without the HPHA process. (a, d) $I_{DS}-V_G$ curves of a representative device that exhibits the hysteretic behavior (at V_{DS} = 0.1, 0.4, 0.7, and 0.1 V). (b, e) Hysteresis window width variation with increasing V_G sweep range in $I_{DS}-V_G$ curves (at V_{DS} = 0.1 V). (c, f) The statistical spread of the hysteresis window widths as a function of the V_G sweep range. V_G sweep rate = ~3 V/s.

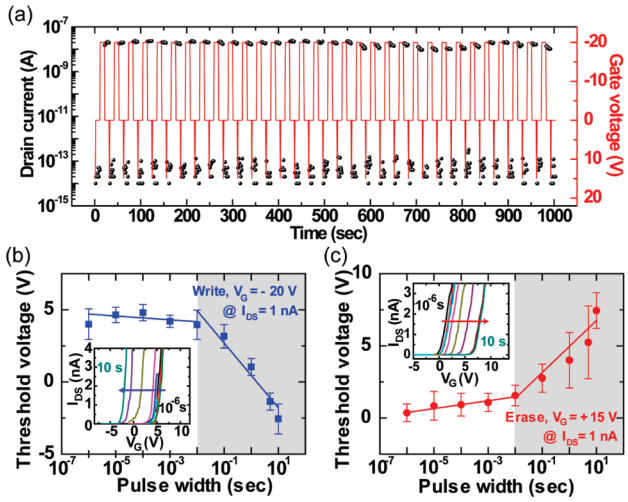

Figure 3. Representative ON/OFF switching characteristics and the statistical data of threshold voltage shifts as a function of pulse width for the nanowire memory devices. (a) The ON and OFF states measured at the read voltage (V_G = 0 V) after write pulses of −20 V for 10 s and an erase pulse of 15 V for 1 s were applied, respectively. The threshold voltage shift as a function of pulse width for (b) the write operation (V_G = −20 V) and (c) the erase operation (V_G = 15 V). The insets show the representative I_{DS}−V_G curves that derive from the application of write (b) and erase (c) pulses with increasing pulse widths, respectively.

nanowire memory FETs were observed to be 3.0 ± 2.6, 9.4 ± 3.5, 15.7 ± 4.3, and 20.7 ± 6.7 for the V_G sweep ranges of 15 V (from −10 to 5 V), 25 V (from −15 to 10 V), 35 V (from −20 to 15 V), and 45 V (from −25 to 20 V), respectively. Note that the hysteresis width was somewhat arbitrarily defined as the difference in the gate voltage at which the drain current (I_{DS}) is 1 nA during the forward and reverse sweeps (Figure 2a,d). It is well known that the hydrogen annealing can generate protons in a SiO_2 layer through hydrogen diffusion in the poly-Si/SiO_2/Si configuration and that the generated protons have mobile characteristics that depend on the applied gate electric field.[24] Therefore, this result suggests that the movement of protons by the application of a gate bias enables the ZnO nanowire FET to exhibit reproducible hysteresis loops.

To investigate the hysteretic nature of nanowire memory FET devices as a potential memory operation, the fabricated transistors were biased with a negative gate voltage (V_G = −20 V, write) and a positive gate voltage (V_G = 15 V, erase). Figure 3a displays the representative data of the reversible ON/OFF switching characteristics of a nanowire memory FET device for pulse signals of V_G = −20 and +15 V at V_{DS} = 0.1 V (also see Figure S1 in the Supporting Information for pulse signals of V_G = ±15 V at V_{DS} = 0.1 V). Here, the interesting result is that, after the application of the write and erase voltage pulses, two memory states, a high conductance (ON state) and a low conductance (OFF state) at V_G = 0 V, were achieved. Importantly, the reversible conductance modulation of the nanowire memory devices implies that the generated protons can repeatedly move between the Si/SiO_2 interface and the SiO_2/ZnO nanowire interface with alternating gate bias polarity. Figure 3b,c shows the distribution of the threshold voltage (defined here as the gate voltages at I_{DS} = 1 nA) as a function of pulse width for four different devices and the corresponding representative I_{DS}−V_G data (the insets of Figure 3b,c) for the application of the write pulse (−20 V) and the erase pulse (+15 V), respectively. The pulse time dependencies of the threshold voltage (V_{th}) shift show two different slopes for both the write and the erase operations. Specifically, when applying a short time pulse (from 1 μs to 10 ms), the V_{th} shift exhibited a weak dependency on the pulse time (with less steep slopes), whereas when applying a relatively longer time pulse (>10 ms), the V_{th} shift exhibited a strong dependency on the pulse time (with much steeper slopes). This indicates that the V_{th} shift is related to the write/erase time scale required to move the protons through the SiO_2 layer (100 nm). Therefore, the switching speed of the nanowire memory FETs is also limited by the movement of mobile protons, which depends on the oxide thickness (t_{ox}) and the gate voltage (V_G). The rate of proton motion across the SiO_2 layer is proportional approximately to V_G^2 and t_{ox}^{-3}.[24] This indicates that write and erase speeds for the devices with a relatively thicker (100 nm) SiO_2 layer are much slower than those in devices with a thinner oxide layer.

In addition to the reversible switching characteristics, we investigated the endurance and retention characteristics of the nanowire memory FETs in order to elucidate the memory functionality that results from the mobile proton-induced hysteresis behavior, compared with the case for the conventional nanowire FETs. Figure 4a,c shows device endurance as a function of the ON/OFF cycles for the nanowire memory FETs and the conventional nanowire FETs, respectively. Here, we observed that the nanowire memory devices exhibit highly reproducible hysteresis loops with well-separated ON and OFF states for hundreds of cycles without degradation at the read voltage (V_G = 0 V at V_{DS} = 0.1 V) (Figure 4a), whereas the conventional nanowire FETs exhibit no memory window between both the ON and the OFF states during the measured hundred cycles. The retention characteristics of the nanowire memory and conventional devices were also measured at the read voltage (V_G = 0 V) after applying a gate bias pulse of −20 V for 10 s (ON state) and +15 V for 1 s (OFF state), as shown in Figure 4b,d, respectively. Interestingly, for the nanowire memory FET devices, the ON and OFF states were well-maintained up to 1000 s in comparison to the conventional nanowire FET devices. Note that the large driving voltages and poor retention properties may be related to the nature of mobile protons in the thick SiO_2 layer (100 nm). Nevertheless, this study can be a proof-of-concept of the nonvolatile memory functionality of the ZnO nanowire FETs.

It is well known that ZnO nanowire FETs are highly sensitive to the presence and nature of adsorbed surface species, such as oxygen or water molecules.[26,27] For example, the influence of the measurement environment has been previously observed to play a dramatic role on the transport properties of ZnO nanowire FETs. In particular, the threshold voltage (V_{th}) shift and hysteresis in electrical properties of ZnO nanowire FET devices can be caused by the adsorbed molecules.[15,28] Therefore, to investigate whether the observed nonvolatile memory behavior is influenced by water and gas molecules in air environment, we further studied the hysteresis and retention properties of a nanowire memory FET in a N_2-filled environment. We similarly observed a remarkable hysteresis memory window and a well-maintained data retention characteristic for the nanowire memory devices in comparison to those in an air environment (see Figure S3 in the Supporting Information). Accordingly, we believe that the nonvolatile memory functions primarily originate from the mobile proton-induced interface effects, but not simply from water or other gas molecules.

The operating mechanism of nanowire memory FETs can be explained by the equilibrium energy band diagrams that correspond to the write/erase operations in the reversible electrical transport properties ($I_{DS}-V_G$), which was characterized after a polychloro-*para*-xylylene (parylene-C) passivation layer was coated so as to effectively remove the influences of gas molecules, such as water or oxygen molecules.[13,15,29] Figure 5a shows the reversible transfer characteristics ($I_{DS}-V_G$) of the nanowire memory devices with a high conductance state (ON state, denoted as (b)) and a low conductance state (OFF state, denoted as (c)) at the read voltage (V_G = 0 V) after applying gate bias pulses of −20 and +20 V, respectively. The operation mode of the devices switched from a write operation into an erase operation after a positive gate bias pulse (V_G = 20 V) was applied and reversely switched from an erase operation into a write operation after a negative gate bias pulse (V_G = −20 V) was applied. The equilibrium energy band diagrams of a nanowire memory device that correspond to the write operation (ON state) and the erase operation (OFF state) in the $I_{DS}-V_G$ curves (Figure 5a) are shown in Figure 5b,c, respectively. For the write operation (ON state), the mobile protons move to the Si/SiO_2 interface after the application of a negative gate bias pulse, resulting in an enhancement of the effective gate electric field. Such a constructive electric field leads to an increase in the channel conductance, a smaller surface depletion, and a relatively lower surface barrier potential at the SiO_2/ZnO nanowire interface (Figure 5b, top). In contrast, for the erase operation (OFF state), the mobile protons move toward the SiO_2/ZnO nanowire interface after the application of a positive gate bias pulse, resulting in the electrostatic capture of electrons at the ZnO nanowire surface (Figure 5c, top). The formation of such interface states can

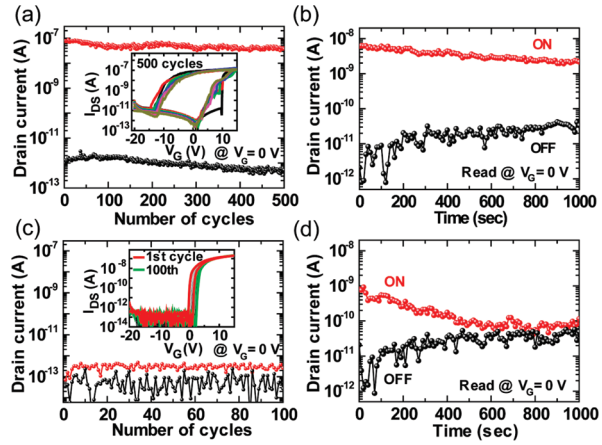

Figure 4. (a, c) Endurance characteristics of a nanowire memory device and a conventional nanowire FET at the read voltage (V_G = 0 V at V_{DS} = 0.1 V), respectively. (b, d) Retention characteristics of a nanowire memory device and a conventional nanowire FET at the read voltage (V_G = 0 V at V_{DS} = 0.1 V) after the application of a write pulse (−20 V, 10 s) and an erase pulse (+15 V, 1 s) respectively. The insets show the hysteresis curves that result from double sweeps of the gate voltage in endurance tests.

reduce the number of free electron carriers of the ZnO surface, as well as create a relatively larger surface depletion width and a higher surface barrier potential, resulting in a shift of the threshold voltage toward the positive gate bias direction and conductance modulation.

Correspondingly, the memory-switching behavior of the nanowire memory FETs can be explained by

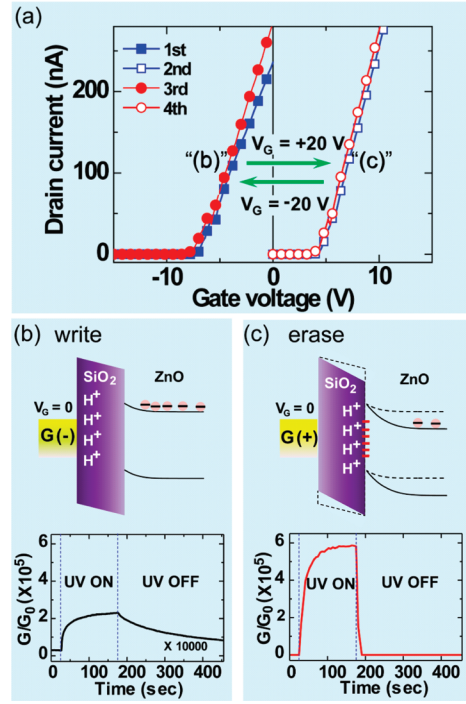

Figure 5. Nonvolatile memory operating mechanism of the nanowire memory devices. (a) Reversible $I_{DS}-V_G$ characteristics after the application of write (V_G = −20 V) and erase (V_G = +20 V) pulses. (b, c) The energy band diagrams at V_G = 0 V after applying write/erase pulses (top) and UV photoresponse characteristics (bottom) that correspond to (b) write and (c) erase operations.

quantitatively considering the concentration of mobile protons, the electrostatically trapped charge concentration, and the effective gate electric field. First, according to secondary ion mass spectroscopy (SIMS) data (Figure S4 in the Supporting Information), the concentration of mobile protons per unit area in the SiO_2 layer can be estimated to be on the order of $\sim 10^{12}$ cm^{-2}, which is consistent with previously reported values.[24,30] In addition, as shown in Figure 5a, changes in threshold voltages ($\Delta V_{th} = \sim 11.5$) can be used to calculate the change in carrier concentration per unit area (Δn_e). Here, for convenience of discussion and simplification, we assume that the Δn_e is equivalent to the electrostatically trapped charge concentration (N_{it}) per unit area at the SiO_2/ZnO nanowire interface using the following equations[13,15,31,32]

$$q\Delta n_e = \frac{C_g \Delta V_{th}}{2\pi r L} \approx qN_{it} \quad (1)$$

$$C_g = \frac{2\pi\varepsilon_{SiO_2} L}{\cosh^{-1}\left(1 + \frac{h}{r}\right)} \quad (2)$$

where C_g is the gate capacitance, r is the nanowire radius (50 nm), L is the nanowire channel length (3 μm), h is the SiO_2 thickness (100 nm), and ε_{SiO_2} is the permittivity of SiO_2 (3.9). Thus, the N_{it} can be estimated to be $\sim 2.8 \times 10^{12}$ cm^{-2}, which is comparable to the concentration of the mobile protons that was determined *via* SIMS characterization. These data indicate that the positively charged protons can capture the electrons electrostatically at the SiO_2/ZnO nanowire interface. These trapped charges at the interface can be expressed as[13,15,31]

$$\Delta Q_d = -\sqrt{2\varepsilon_{ZnO} q N_d \Delta\phi_S} = -qN_{it} \quad (3)$$

where ΔQ_d is the change in the depleted amount of areal charge density in the ZnO nanowire, ε_{ZnO} is the permittivity of ZnO (8.66), N_d is the doping concentration, and $\Delta\phi_S$ is the change in the surface barrier potential. In addition, the effective gate electric field at the ZnO nanowire surface can be calculated from the following equation[15,33,34]

$$\xi_{eff} = \frac{1}{\varepsilon_{ZnO}}\left(\frac{1}{2}Q_{tot} + Q_d\right) \quad (4)$$

where Q_{tot} is the total areal charge density in the ZnO nanowire channel. Here, if we assume $\phi_S = 0.01$ V (for the write operation) and $N_d = 5 \times 10^{17}$ cm^{-3} as typical values, then we can obtain $\phi_S = 0.42$ V (for the erase operation) and $\zeta_{eff} = 0.87$ and 0.03 MV/cm at $V_G = 10$ V for the write and erase operations, respectively, using eqs 1−4 (also see Figure S5 in the Supporting Information). This implies that the nonvolatile memory-switching behavior in the nanowire memory FETs is caused by the modulation of the interfacial properties, including the effective gate electric field, surface charge density, and surface barrier potential.

Furthermore, to unambiguously explain the impact of the electrostatically trapped charges at the SiO_2/ZnO nanowire interface due to mobile protons, we investigated the UV photoresponse of a nanowire memory device that corresponds to the write operation (ON state) and the erase operation (OFF state) in the $I_{DS}-V_G$ curves (Figure 5b,c, bottom, respectively). Note that the normalized photoconductance response was plotted for the ratio of the conductance measured when the UV was on (G) and off (G_0). Interestingly, as shown in the photoconductance responses (Figure 5b,c, bottom; also see Figure S6 in the Supporting Information), we found that the UV sensitivity of the ZnO nanowire for the erase operation was much higher than that for the write operation. This is likely caused by the negative interface states arising from the electrons trapped electrostatically by the protons that moved toward the SiO_2/ZnO nanowire interface after the application of a positive gate bias pulse. The presence of the negatively charged species, such as oxygen molecules or immobilized electrons, highly sensitize the UV detection of a ZnO nanowire.[35,36] Similarly, upon UV illumination, the electrons that are electrostatically trapped by the positively charged protons can act as photon-generated hole-trapping states, resulting in a highly sensitive UV response. It is immediately apparent that the modulation of the interfacial properties is caused by the movement of protons *via* the applied gate electric field, resulting in the nonvolatile functionality of ZnO nanowire FETs.

CONCLUSION

In summary, we have fabricated the ZnO nanowire-based nonvolatile memory FETs using mobile protons, which can be generated by the high-pressure hydrogen annealing (HPHA) at low temperature (400 °C). The nanowire memory FET devices exhibited reproducible hysteresis behavior, stable ON/OFF switching, and nonvolatile memory characteristics. The memory functionality of ZnO nanowire transistors can be explained in terms of the modulation of interfacial properties, such as the effective gate electric field, surface charge density, and surface barrier potential, due to the movement of protons in the SiO_2 layer that is caused by the application of a gate electric field.

EXPERIMENTAL METHODS

Device Fabrication. The detailed method of ZnO nanowire growth by vapor transport and the general fabrication method of nanowire FETs are described elsewhere.[13] To generate mobile protons in the SiO_2 layer (100 nm), the hole patterned substrate (poly-Si (50 nm)/SiO_2 (100 nm)/highly doped p-type Si substrate) was placed into a chamber and annealed in pure hydrogen environment under a pressure of 10 atm and at a temperature of

400 °C for 40 min. After the substrates were annealed, the chamber was cooled at the room temperature.

Passivation Layer Coating. To effectively remove the influence of water or gas molecules in ambient air, a passivation layer of parylene-C film (dielectric constant $\varepsilon = 3.1$ at 1 kHz) was deposited on fabricated devices at room temperature by vacuum sublimation in a special coating system (Labcoater 2010, U.K.).[29]

Device Characterization. The measurement of the memory characteristics for the fabricated devices was carried out using a semiconductor parameter analyzer, HP 4145C. In addition, a Keithley 4200 semiconductor characterization system was used to measure the electrical characteristics of nanowire FETs in a N_2-filled ambient, as well as their UV photoresponse.

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Supporting Information Available: ON/OFF switching, nonvolatile characteristics in N_2-filled ambient, and UV photoresponse of ZnO nanowire memory devices; quantitative estimation of surface barrier potential, surface charge density, and effective electric field for the device; and hydrogen depth profile using secondary ion mass spectroscopy (SIMS). This material is available free of charge *via* the Internet at http://pubs.acs.org.

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